METHOD AND APPARATUS FOR HOT CARRIER PROGRAMMED ONE TIME PROGRAMMABLE (OTP) MEMORY

Field of the Invention

The present invention relates generally to integrated circuits including electronic memory devices, and more particularly to one time programmable (OTP) memories.

Background of the Invention

One time programmable (OTP) memories are often used to store program code and other information. Among other benefits, the one-time nature of OTP memories prevent authorized program code from being modified or over-written with unauthorized program code. OTP memories may be implemented, for example, using are fusible links, antifuse or floating gate non-volatile memory technologies. Fusible links are metal or polysilicon wires that are "blown," i.e., made to have higher resistance, by passing a high current through them. As a result, fusible links exhibit some amount of physical destruction of the metal or polysilicon wire. Fusible links are relatively large and require relatively high current to program. Antifuse is the partial physical destruction or degradation of a Metal Oxide Semiconductor (MOS) capacitor gate oxide dielectric by the application of a high voltage. A lower resistance conduction path is formed between the plates of the capacitor through the oxide dielectric. Antifuse technologies require relatively high voltage to program and do not scale well with Complementary Metal Oxide Semiconductor (CMOS) technologies. The thinner MOS gate oxides associated with current CMOS technologies do not program consistently in a reliable manor.

Floating gate non-volatile memory involves the injection of electrical charge onto the isolated or unconnected (floating) gate of a field-effect-transistor (FET). The accumulation of charge on the gate changes the threshold voltage of the transistor, which can be sensed during a read operation. Floating gate non-volatile memories are employed for "flash" non-volatile memories. Floating gate non-volatile memories require relatively high voltage and sometimes relatively high current to program. Furthermore, floating gate non-volatile memories usually require additional special CMOS processing, thereby increasing fabrication cost.

A need therefore exists for improved OTP memories that are small in size and can be programmed with low voltages and small current.

Summary of the Invention

Generally, one time programmable memory devices are disclosed that are programmed using hot carrier induced degradation to alter one or more transistors characteristics. A one time programmable memory device is comprised of an array of transistors. Transistors in the array are selectively programmed using hot carrier induced changes in one or more transistor characteristics, such as changes to the saturation current, threshold voltage or both, of the transistors. The changes to the transistor characteristics are achieved in a similar manner to known hot carrier transistor aging principles. The present invention recognizes that such characteristic changes can be selectively applied to memory cells in OTP memory devices in order to program the OTP memory device in a desired manner.

The present invention provides for small, low cost, OTP memories that are programmable at low voltages and small current. The OTP memories of the present invention can be fabricated with normal CMOS processing techniques with little, if any, additional processing steps and with minimal, if any, increased fabrication costs. The OTP memories of the present invention are scalable with future CMOS technologies.

A more complete understanding of the present invention, as well as further features and advantages of the present invention, will be obtained by reference to the following detailed description and drawings.

Brief Description of the Drawings

FIG. 1 illustrates a conventional fusaible link or antifuse OTP memory array;

FIG. 2 illustrates an OTP memory array incorporating features of the present invention;

FIG. 3 is a schematic diagram illustrating the various terminals of each memory cell of FIG. 2;

FIG. 4 is a cross-sectional view of a typical MOS FET transistor;

FIGS. 5A and 5B are schematic diagrams illustrating the programming and reading, respectively, of a first embodiment of an OTP memory cell incorporating features of the present invention; and

FIGS. 6A and 6B are schematic diagrams illustrating the programming and reading, respectively, of a second embodiment of an OTP memory cell incorporating features of the present invention.

Detailed Description

FIG. 1 illustrates a conventional two by two fusible link or antifuse OTP memory array 100 of memory cells 110-1,1 through 110-i, j. The memory cells 110-1,1 through 110-i, j are generally comprised of FET transistors in series with the fusible element generally arranged in a grid pattern having a plurality (or series) of rows and columns. As shown in FIG. 1, the exemplary OTP array 100 includes a plurality, i, of rows (i=2), and a plurality, j, of columns (j=2). Each column is supplied with power at a first predetermined voltage level, often referred to as the "pre-charged voltage level," and each row is supplied with power at a second predetermined voltage level. Values for these first and second predetermined voltage levels typically depend upon the selected implementation.

As shown in FIG. 1, a gate of each transistor 110 of the OTP array 100 is connected to a particular row of the series of rows. A source of each transistor is generally programmably connected to ground through the fuse element and a drain of each transistor is connected to a particular column of the series of columns. The fusible element can be a fusible link or an antifuse. A fusible link is programmed by passing current through the link of sufficient magnitude and duration to change the electrical properties of the link from low to high resistance. An antifuse is programmed by applying a voltage across the antifuse of sufficient magnitude to change its electrical characteristics from high to low resistance. The programming current or voltage for the fusible link or antifuse may be routed through the illustrated cell transistor or through additional transistors not shown.

FIG. 2 illustrates a two by two OTP memory array 200 of memory cells 210-1,1 through 210-i, j that may, for example, comprise a portion of an integrated circuit. The memory cells 210-1,1 through 210-i, j are generally comprised of FET transistors generally arranged in a grid pattern having a plurality (or series) of rows and columns. FIG. 3 is a schematic diagram illustrating the various terminals of the FET transistor within each memory cell 210 of FIG. 2. As shown in FIG. 2, the exemplary OTP array 200 includes a plurality, i, of rows (i=2), and a plurality, j, of columns (j=2). Each column is supplied with power at a first predetermined voltage level, often referred to as the "pre-

charged voltage level," and each row is supplied with power at a second predetermined voltage level. Values for these first and second predetermined voltage levels typically depend upon the selected implementation.

As shown in FIG. 2, a gate of each transistor 210 of the OTP array 200 is connected to a particular row of the series of rows. A source of each transistor is generally connected to ground and a drain of each transistor is connected to a particular column of the series of columns. According to the present invention, the OTP array 200 is programmed using hot carrier induced changes in transistor characteristics (saturation current, threshold or both).

Hot Carrier Aging

Hot carrier aging is the degradation of transistor characteristics over time caused by the injection of carriers into the gate oxide at the drain end of the device. Carrier injection into the oxide causes oxide damage and creation or filling of traps near the drain. As a result, the channel mobility degrades, causing a decrease in device saturation current. In addition, a localized increase occurs in the device threshold at the drain end of the channel region. Hot carrier transistor degradation can be accelerated so that it occurs in a relatively short time by device optimization or the application of modestly higher drain and gate voltages (or both).

The present invention recognizes that the above-mentioned degradation of transistor characteristics can be used to advantage to program OTP memories. The FET transistors 210 of FIG. 2 can be selectively "programmed" by the application of "stressful" voltage levels to appropriate terminals of the FET transistor in order to introduce hot carrier transistor degradation. These stressful voltage levels could be normal logic voltage levels (V_{DD}) or marginally higher voltage levels. The stressful voltage levels required by the present invention are not as high as those required by other proposed OTP memories and are easily provided using normal logic or input/output transistors and usual circuit design techniques.

After selectively programming transistors 210 in the OTP memory array 200, the programmed transistors 210 will have significantly lower saturation current, or lower threshold voltages at the end of the channel close to where the stress voltage was applied during programming, or both. Thus, programmed cells can be detected during a read operation by either sensing the lower saturation current or by sensing the lower threshold voltage.

FIG. 4 is a cross-sectional view of a typical MOS FET transistor 400 similar to that used for an OTP memory cell. The basic construction and function of the MOS FET transistor 400 is well known. The MOS FET transistor 400 is formed on a silicon substrate 430. Source 450 and drain 440 are formed by relatively heavy implants of impurities. A gate insulator 460, typically silicon dioxide, is formed over the channel region 480. A gate electrode 470, typically poly-silicon, is formed over the gate insulator.

As is well known, there are two general types of MOS FET transistors, n-channel and p-channel types. N-channel transistors are used herein for the purpose of illustration of the present invention. It is recognized that p-channel transistors could also be used for the present invention. As is well known, an n-channel transistor is constructed on a p type substrate, or alternately a p-well, and has n-type impurity implants for source 450 and drain 440.

FIG. 5A is a schematic diagram illustrating the programming of a first embodiment of an OTP memory cell 500 incorporating features of the present invention. The OTP memory cell 500 may be embodied, for example, as a MOS FET transistor. As shown in FIG. 5A, an OTP memory cell 500 is programmed using hot carrier induced changes to the threshold voltage by applying "stressful" voltage levels to the drain (Vd_{stress}) and gate (Vg_{stress}). The hot carrier degradation of the transistor characteristics creates an oxide damage area 510 (traps) near the drain that causes a localized increase in the device threshold at the drain end of the channel region.

FIG. 5B is a schematic diagram illustrating the reading of the OTP memory cell 500 of FIG. 5A. When reading the OTP memory cell 500, the lower saturation current and threshold voltage is most apparent when the transistors current flow is in the opposite direction to current flow during programming. If the drain is defined for purposes of illustration as the terminal that is positive during program operations (FIG. 5A), then the source is the positive terminal during read operations (FIG. 5B). During read operations, the higher threshold channel region is near the grounded drain, so that its higher threshold is not hidden by the positively biased source junction's space charge region.

During a read operation, different sensing techniques and circuits would be used to differentiate programmed cells from non-programmed cells depending upon which transistor characteristic is used. If a cell has been programmed by inducing a change in the cell threshold voltage, such as in the OTP memory cell 500 of FIGS. 5A and 5B, then the cell 500 is read by (i) raising the source terminal for all cells to a positive potential

(V_{DD}); and (ii) raising the gate connection for all cells along the selected row to a positive potential (V_{DD}). The column (drain) voltage would then change from its precharged voltage level (ground) to a cell transistor threshold voltage (Vt) below the source potential (V_{DD}). The programmed cells would have a higher Vt than the non-programmed cells that would be detected by the sense amplifier connected to the column.

FIG. 6A is a schematic diagram illustrating the programming of a second embodiment of an OTP memory cell 600 incorporating features of the present invention. As shown in FIG. 6A, an OTP memory cell 600 is programmed during fabrication using hot carrier induced changes to the saturation current by applying "stressful" voltage levels to the source (Vs_{stress}) and gate (Vg_{stress}). The hot carrier degradation of the transistor characteristics creates an oxide damage area 610 (traps) near the source that degrades the channel mobility, causing a decrease in device saturation current

FIG. 6B is a schematic diagram illustrating the reading of the OTP memory cell 600 of FIG. 6A. If a cell has been programmed by inducing a change in the cell saturation current, such as in the OTP memory cell 400 of FIGS. 6A and 6B, then the cell source terminal would remain at ground. The selected row (gate terminal) would be raised to a positive potential (V_{DD}) and current would be drawn from the precharged high (V_{DD}) column. The column voltage would decay towards ground. The rate of decay would depend upon column capacitance and cell saturation current. Thus, the columns associated with active programmed cells would decay at a slower rate than those associated with non-programmed cells. Sense amplifiers connected to the columns would differentiate between the programmed and non-programmed column voltage decay rates.

In further variations of the present invention, hot carrier programmable transistor cells can be enhanced by tailoring their structure to have more pronounced changes in saturation current and/or threshold voltage, or to have these changes occur at lower programming voltages or during shorter applications of programming voltages. Optimum transistor design for hot carrier effects is well known in the art (e.g., sharp drain junction profiles and non lightly doped drains (LDD)). The junction that receives the stress voltage during programming could be tailored for more pronounced changes in saturation current and/or threshold voltage. The other junction could remain as a common logic transistor junction that is designed to be relatively immune from hot carrier induced changes.

It is to be understood that the embodiments and variations shown and described herein are merely illustrative of the principles of this invention and that various modifications may be implemented by those skilled in the art without departing from the scope and spirit of the invention. For example, the OTP memory cells of the present invention can also be used as non-arrayed storage elements for applications requiring only a few OTP bits. The OTP memory cells of the present invention can also be implemented as multi-level flash or non-volatile cells that store two or more bits per cell. The OTP memory cells of the present invention provide low-cost alternative OTP element that can be used for high and low density applications, such as repair of Static Random Access Memories (SRAMs) and Dynamic Random Access Memories (DRAMs), identification and characterization coding of wafers and chips, analog circuit trimming, electronic fuses, field programmable logic devices, and encryption coded macros or systems.